

LCFC Confidential


Miray-SKY M/B Schematics Document

INTEL SKYLAKE Mobile ULT Platform
INTEL SKY Y-series CPU + LPDDR3 Memory

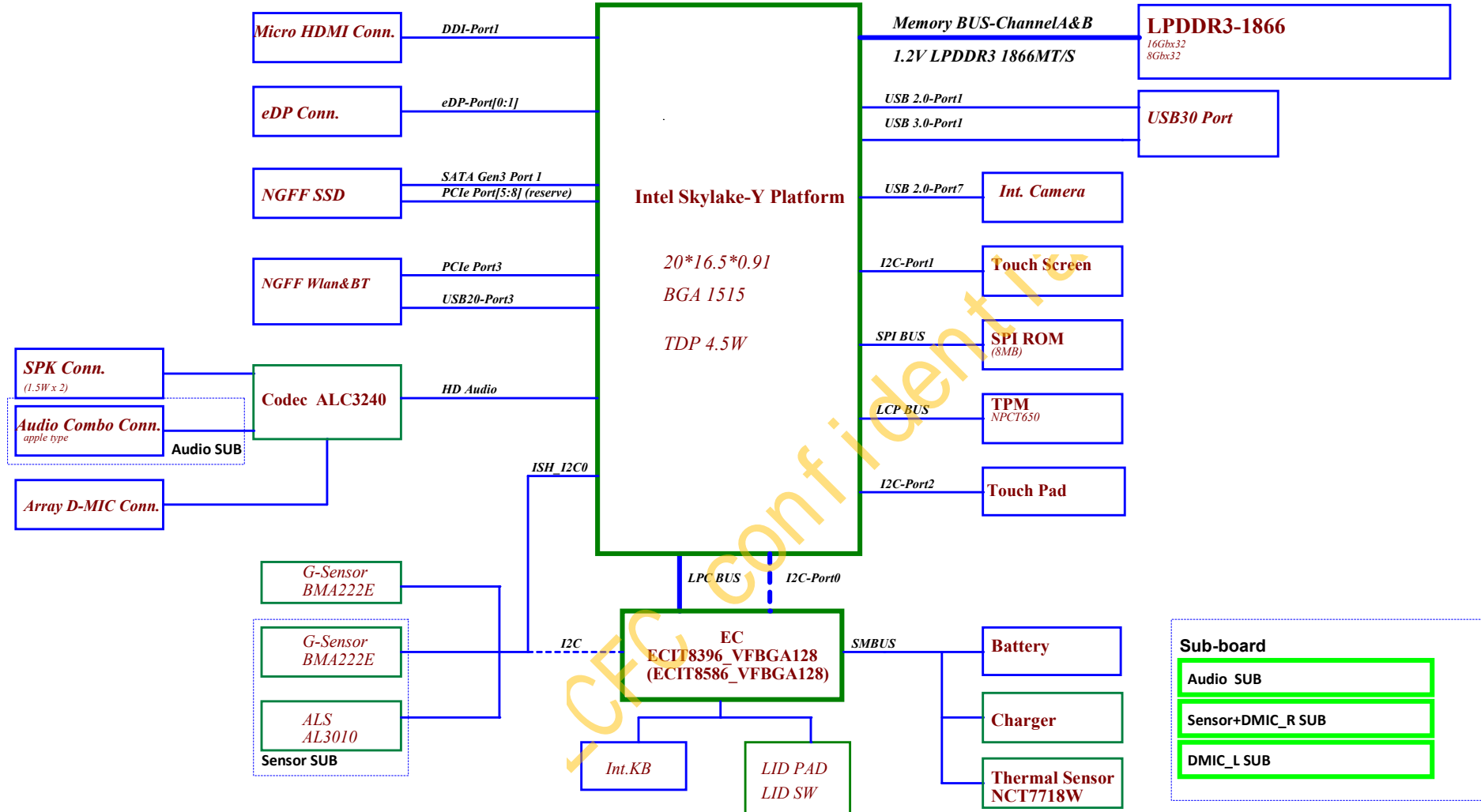
2016-02-17

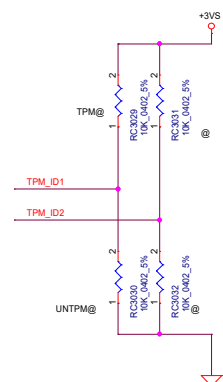
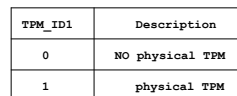
REV:1.0

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/11/09	Deciphered Date	2015/11/09	Cover Page	
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				C	Miray
				Date	Monday, February 29, 2016
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				Rev	1.0

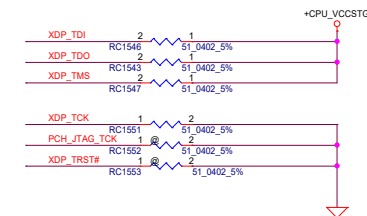
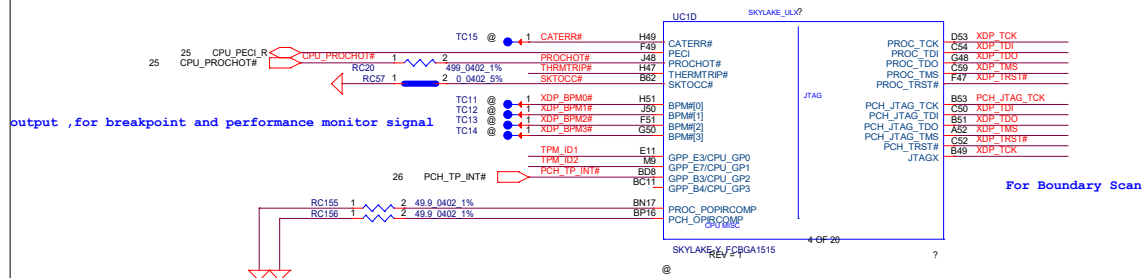


LCFC-Miary Block diagram

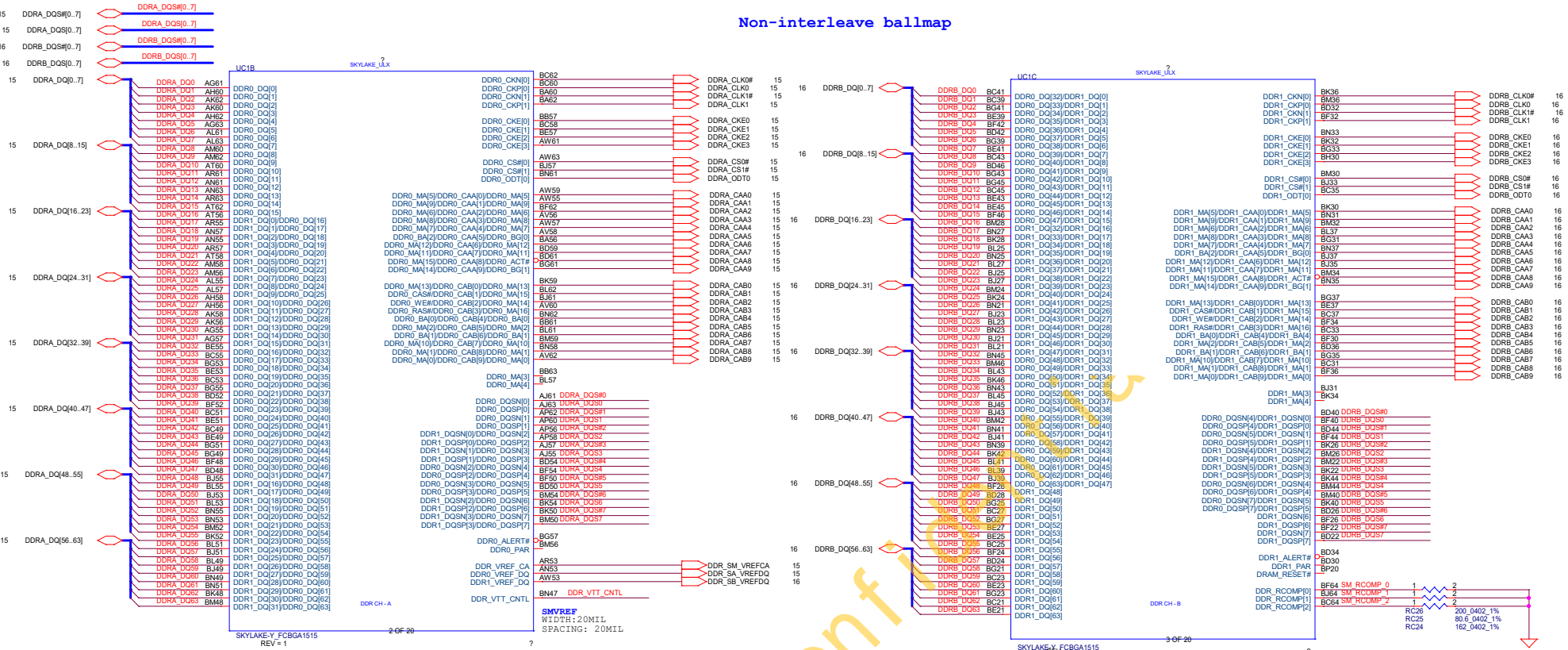




```
0901 add
```



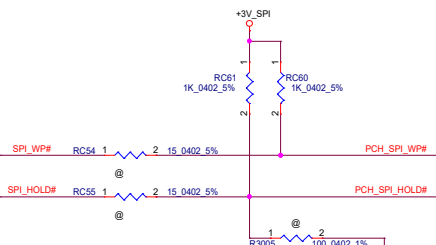
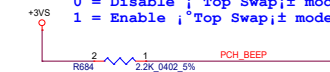
Non-interleave ballmap





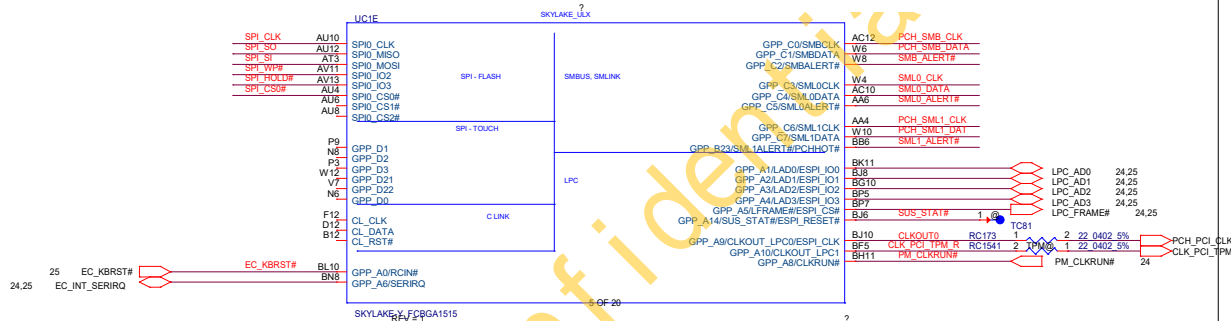
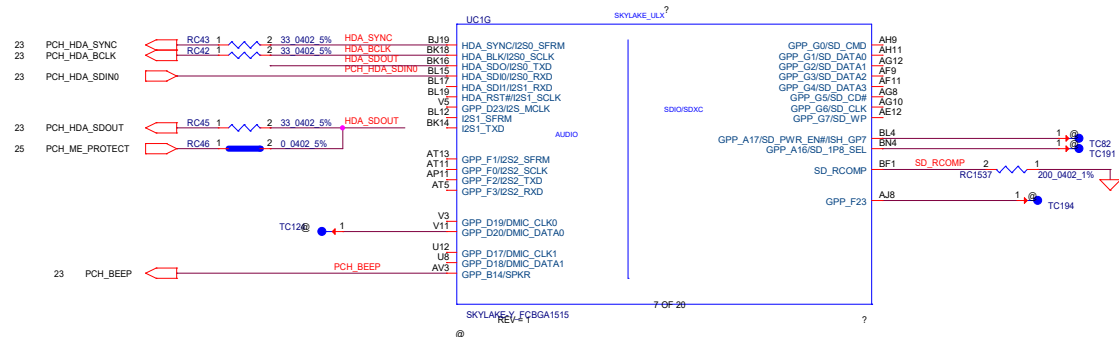
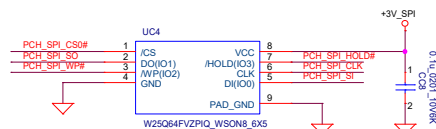
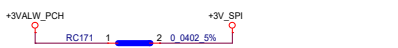
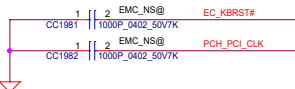
CC7
10P_0402_50V8J

The signal has a weak internal pull-down.
0 = Disable $i^{\circ}\text{Top Swap}i^{\pm}$ mode. (Default)
1 = Enable $i^{\circ}\text{Top Swap}i^{\pm}$ mode.



SPI_HOLD# for SKL ES Sample

- * 2. 100ohm PD, 1K PU, disabled after RSMRST# de-assertion

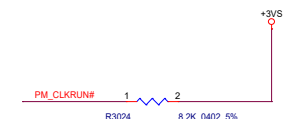
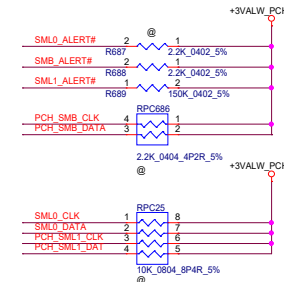





```
for signal SMB ALERT#:
```

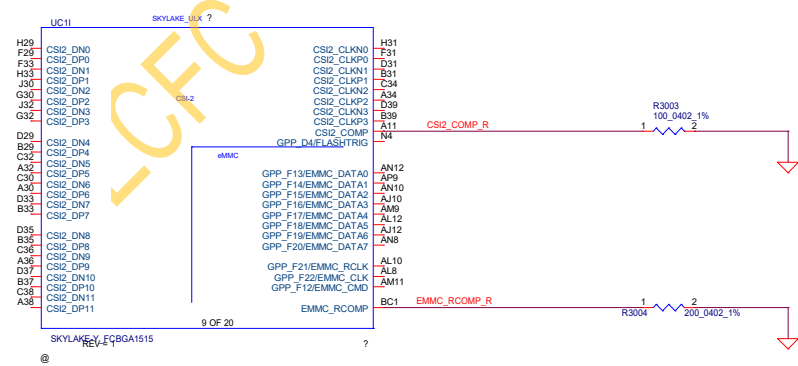
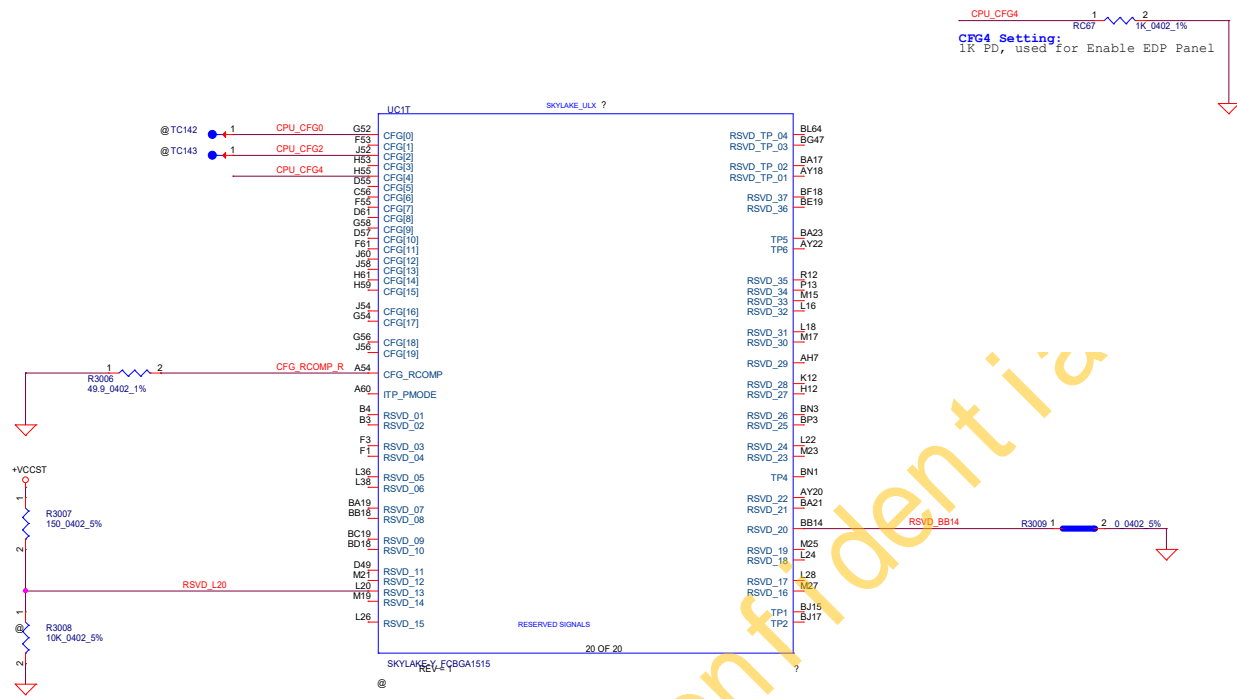
This signal has a weak internal pull-down.

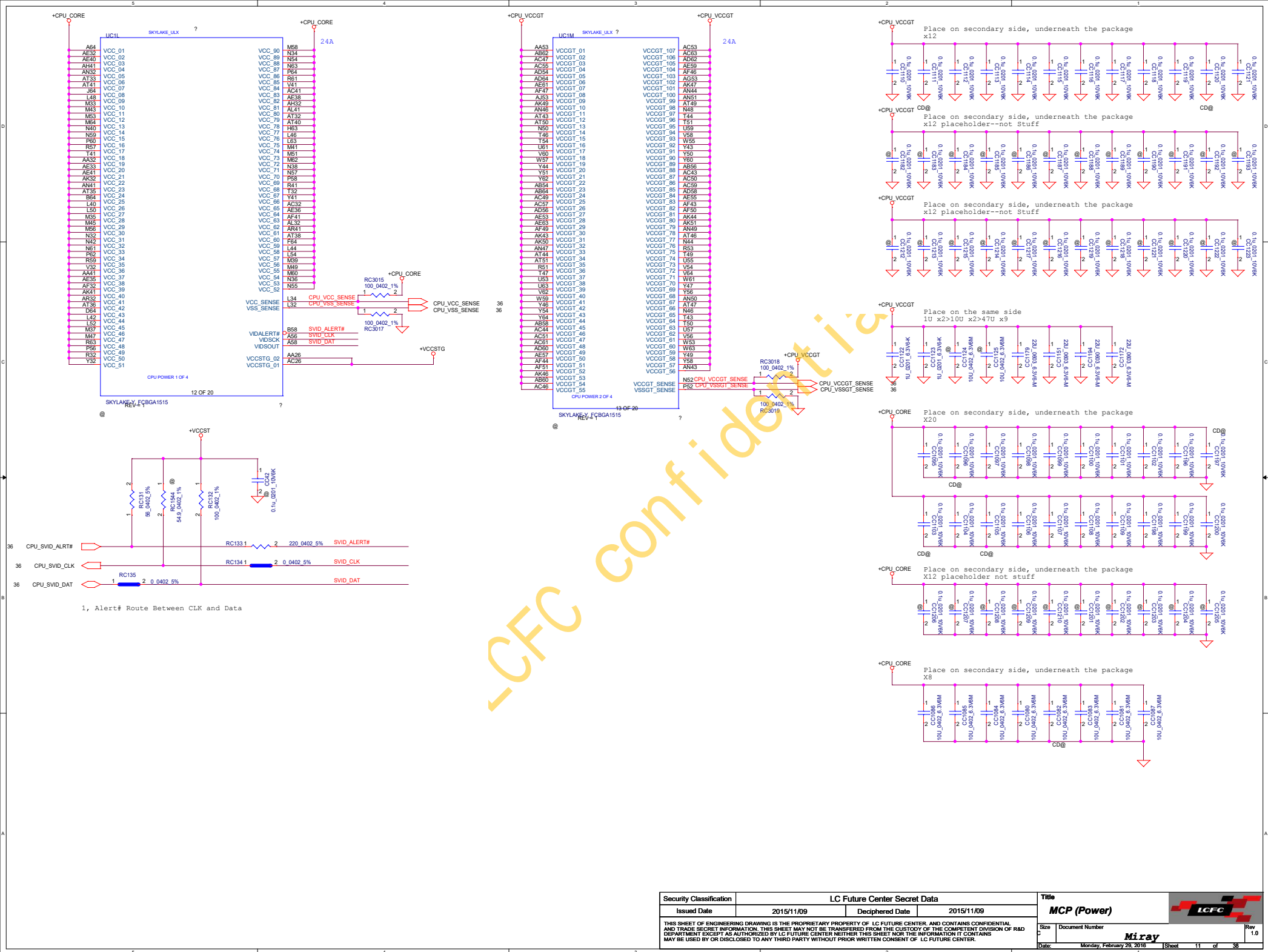
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)


1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

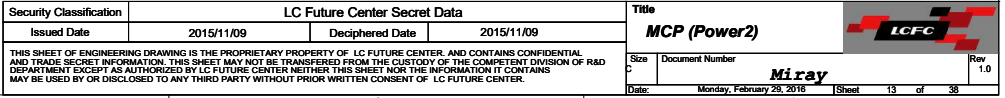


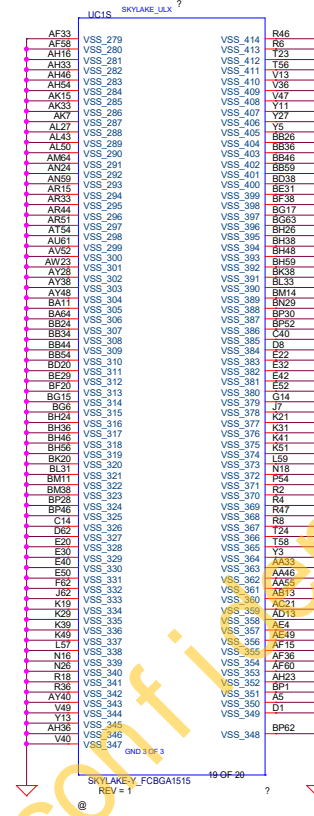
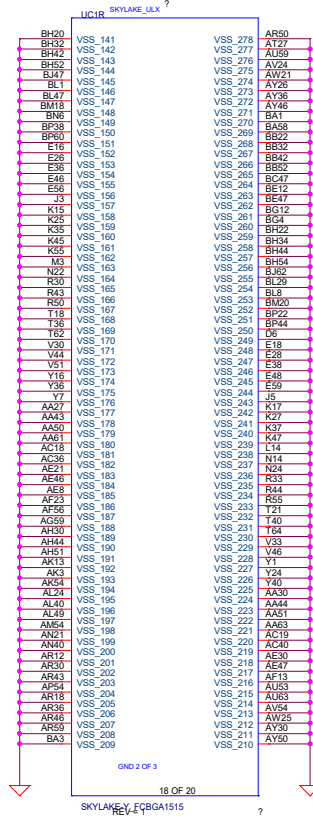
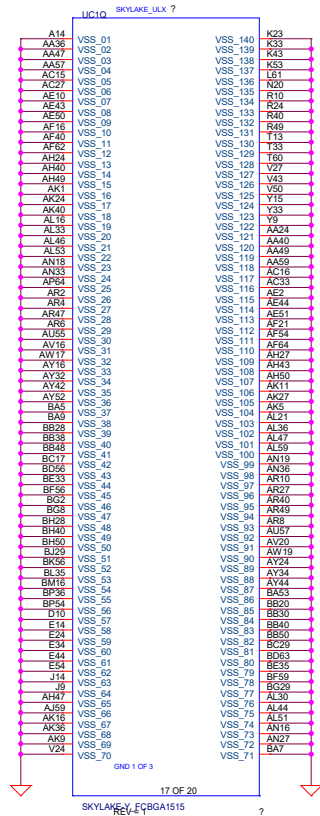
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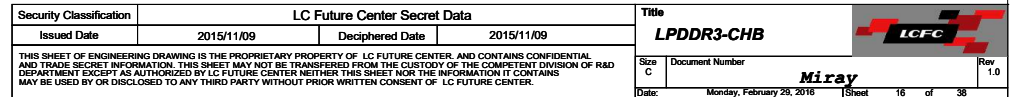




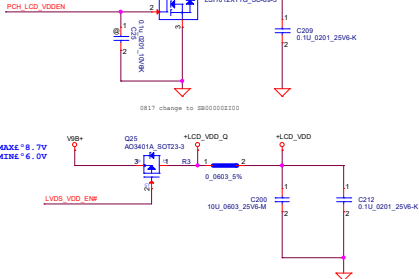
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2015/11/09		2015/11/09		Size C Document Number Miray		Rev 1.0	
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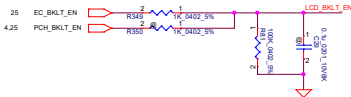


EDP Panel



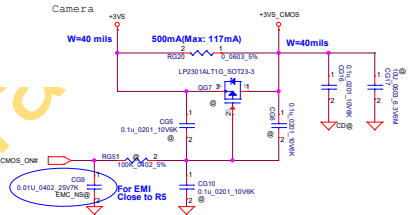
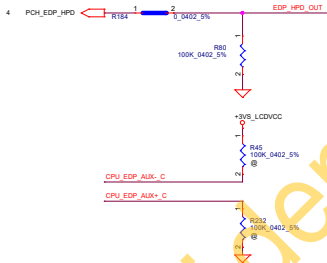
NOTE

1. AC 19V/DC 8.2V
2. AO5800E for VDS concern
3. R235, R237 for VGS concern
4. C200 for voltage concern





FPC:

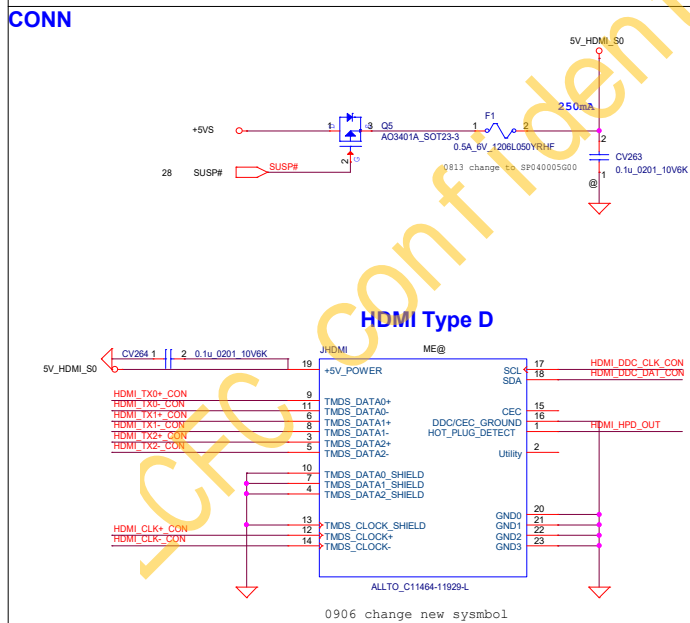
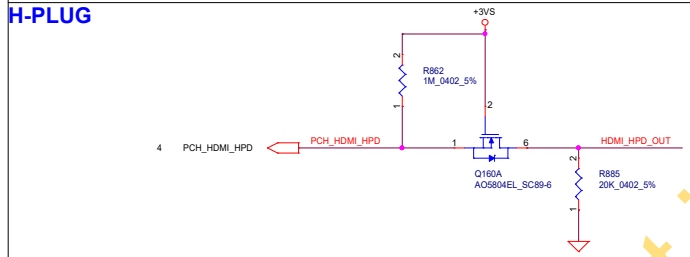
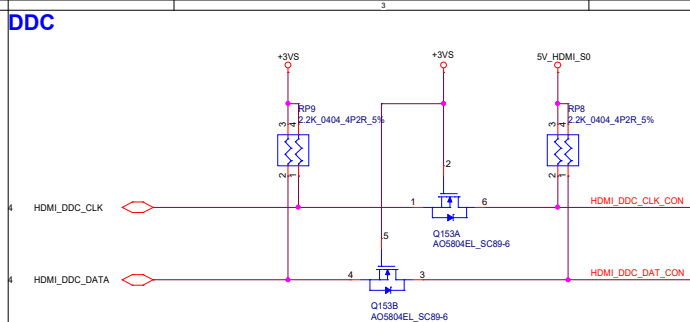
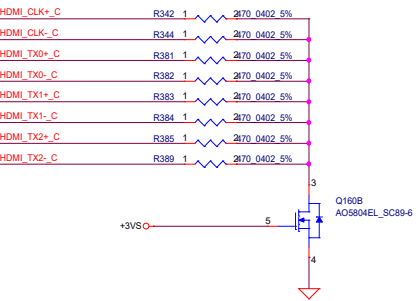
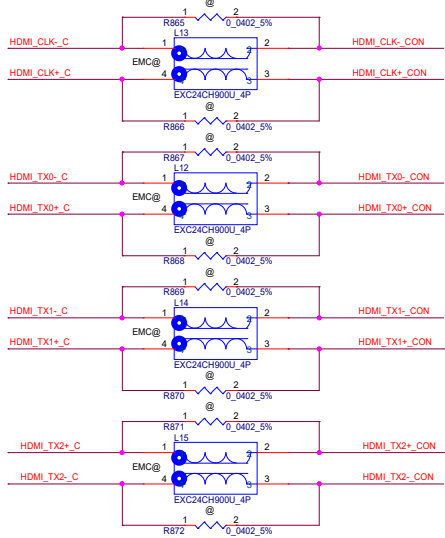
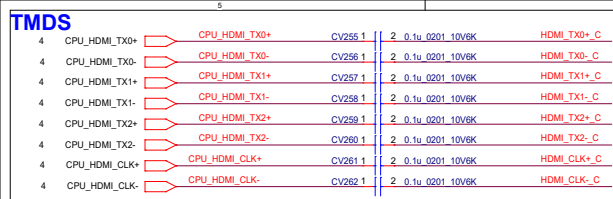
1. pin to pin with EDP Panel, check the panel pin definition
2. check the HSYNC for Touch screen board



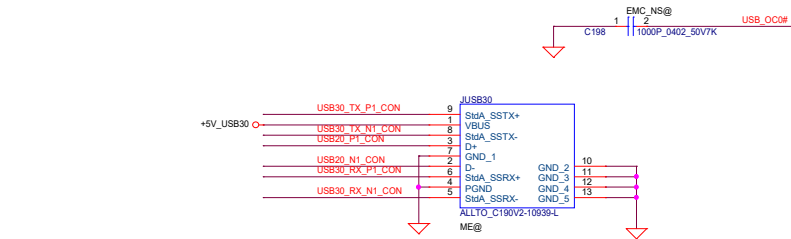
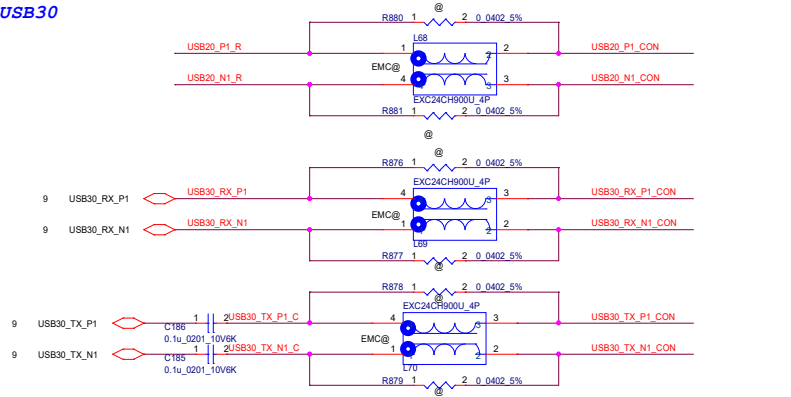
1106 symbol update

Reserve for other function

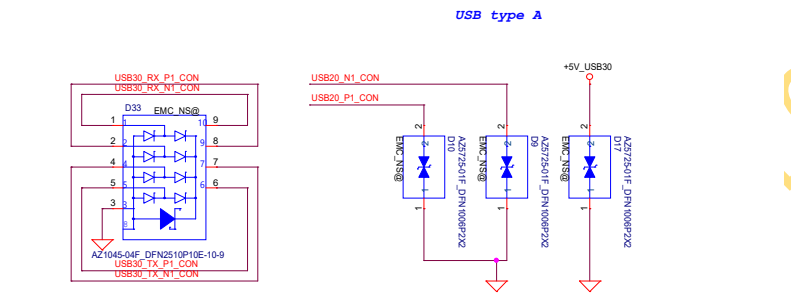
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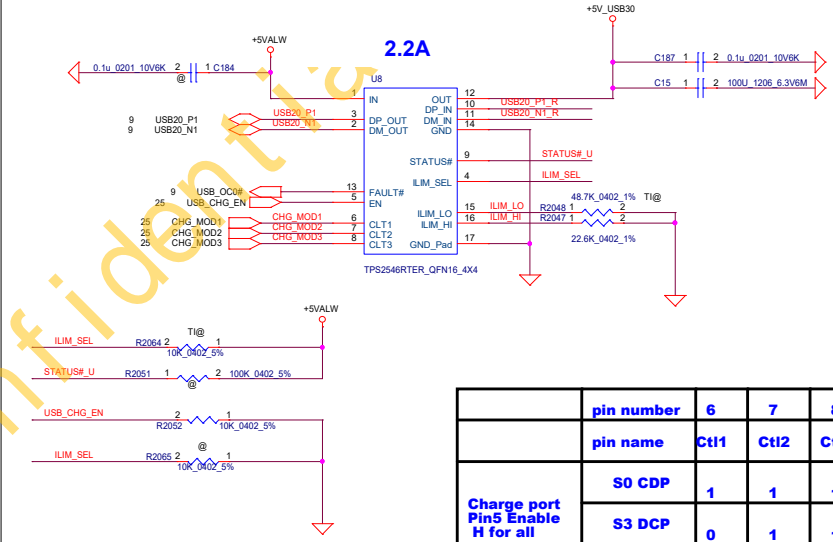
USB30



1105 change new symbol



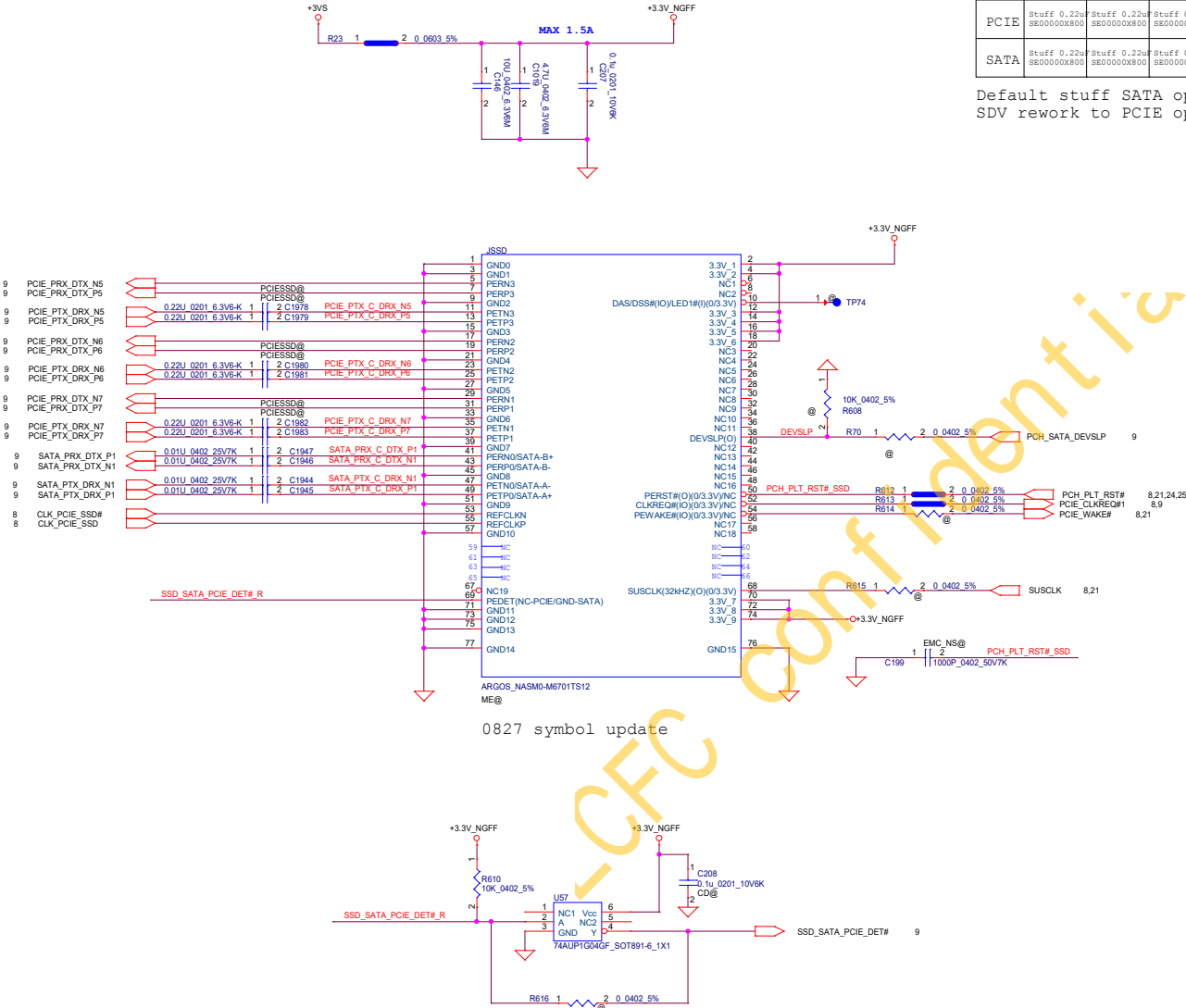
USB charger



	pin number	6	7	8	4
	pin name	Ctl1	Ctl2	Ctl3	ILM_SEL
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

SSD	C1978	C1979	C1980	C1981	C1982	C1983	C1947	C1946	C1944	C1945
PCIE	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0ohm SD02800008J	Stuff 0ohm SD02800008J	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800
SATA	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.22uF SE000000X800	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J

Default stuff SATA option
SDV rework to PCIE option and test SATA/PCIE signal and SSD



Mini Card (WLAN/WiMAX)

The schematic diagram illustrates the internal circuitry of a Mini Card, specifically for WLAN/WiMAX functionality. Key components and connections include:

- Power Management:** +3V5 WLAN, +3V5, and +3V5_WLAN pins are shown with associated decoupling capacitors (e.g., 100K, 0.4402, 5%).
- USB Interface:** USB20_P4 and USB20_M4 pins are connected to the USB module.
- PCIe Interface:** PCE_PTX_DRX_P3, PCE_PTX_DRX_N3, PCE_PTX_DRX_P3, and PCE_PTX_DRX_N3 pins are connected to the PCIe module.
- UART Interface:** UART_TX_DEBUG_R and UART_RX_DEBUG_R pins are connected to the UART module.
- WLAN/WiMAX Interface:** WLAN_CLKREQ, WLAN_WAKEUP, and WLAN_WAKEUP pins are connected to the WLAN module.
- Other Pins:** Various other pins like BT_CTRL, BT_ON#, and PCH_BT_ON# are shown with their respective connections.

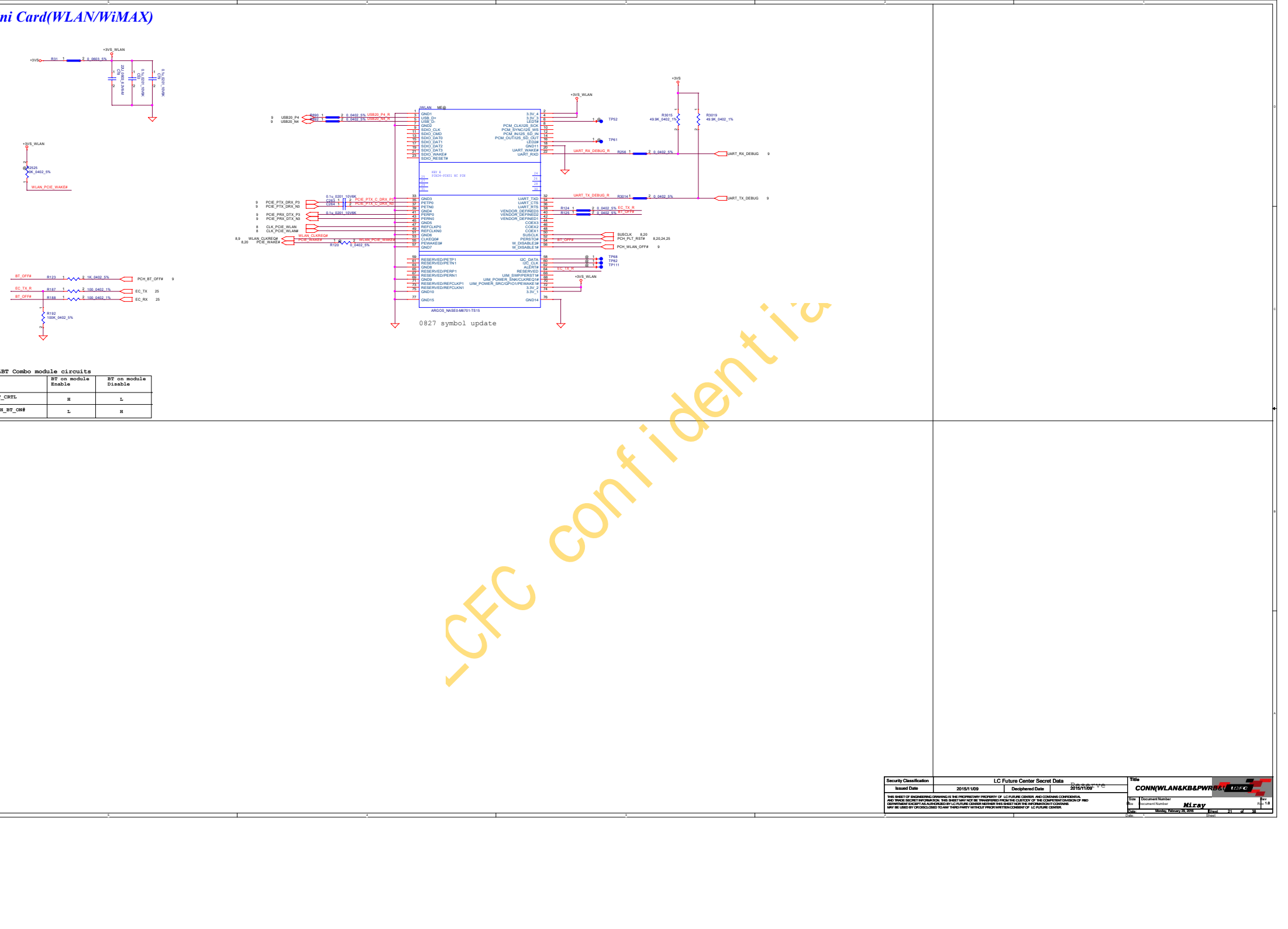
WLAN/BT Combo module circuits

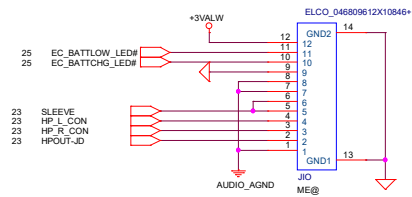
	BT on module Enable	BT on module Disable
* BT_CTRL	H	L
PCH_BT_ON#	L	H

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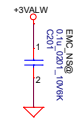
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Revision	1.0	1.0
Author	Miray	Miray
Checker		
Page	21	21

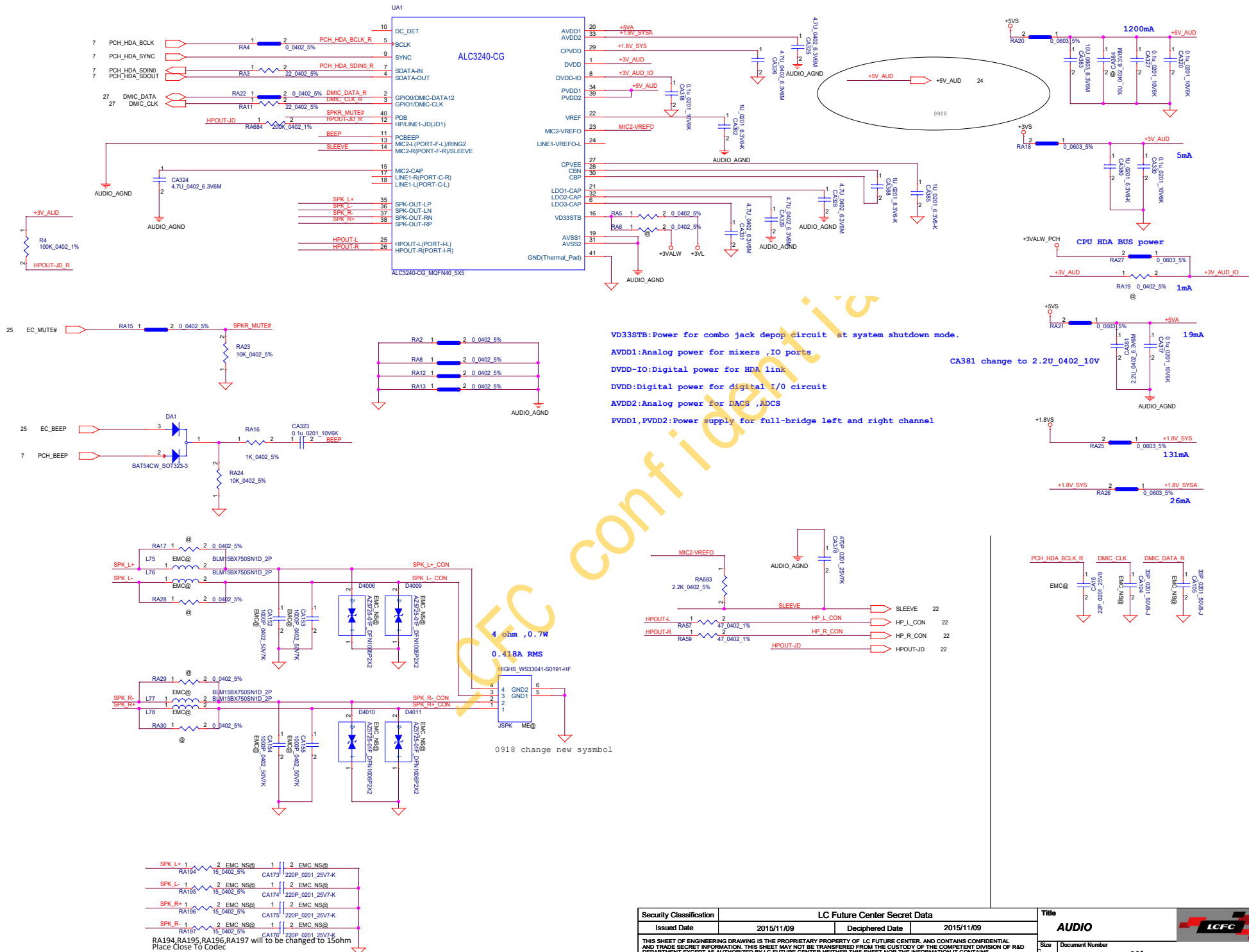
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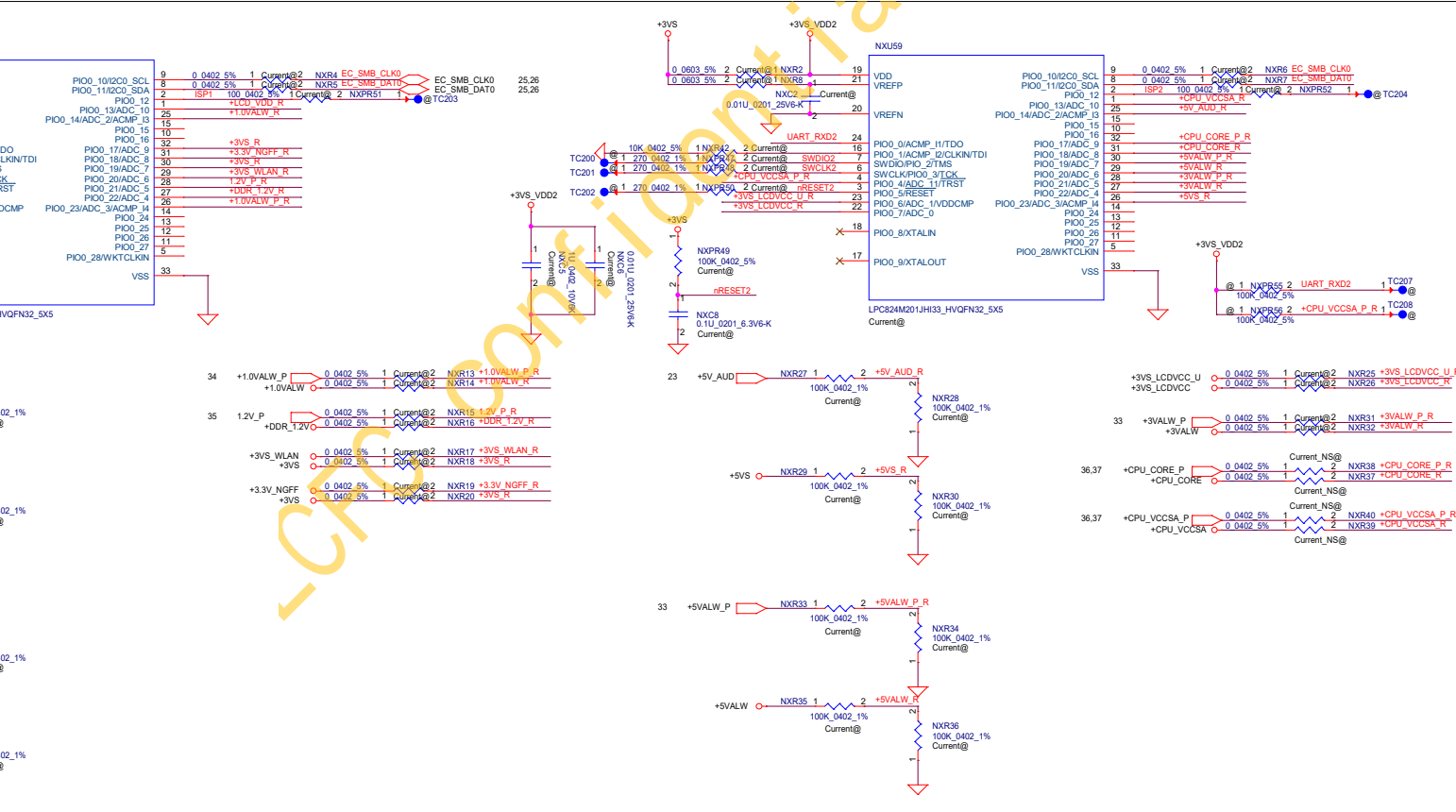
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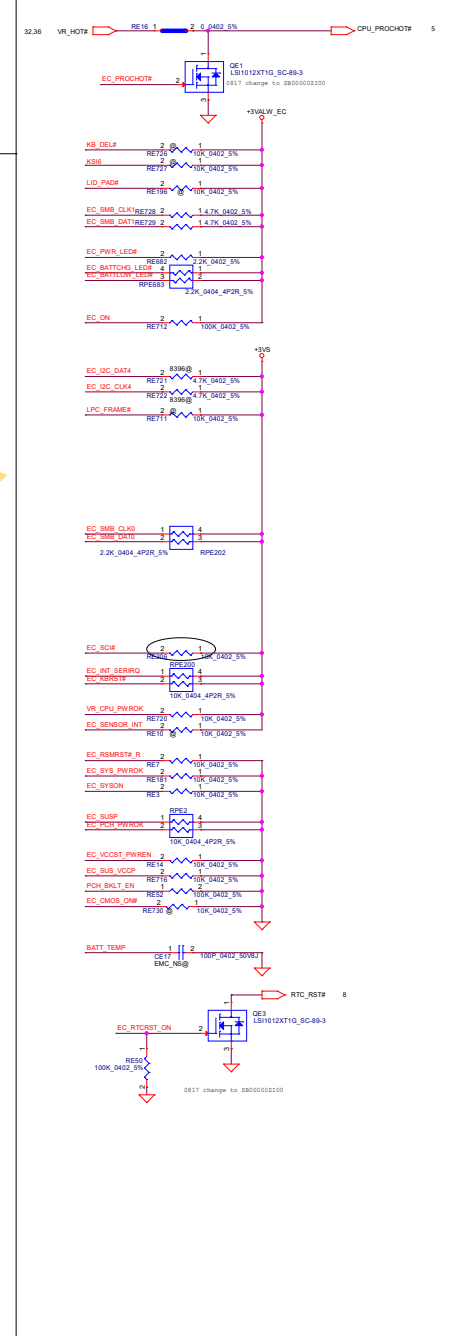


LCFC confidential

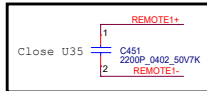


SDV Use WW2.0 Nuvoton
SIV need change to WW1.2 QFN



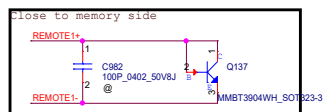
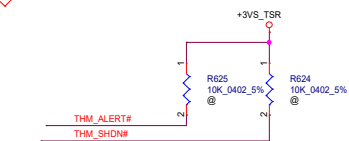
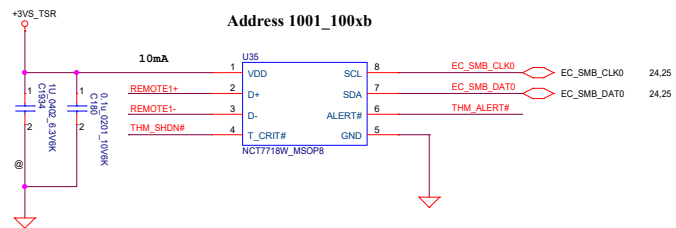


THM Sensor

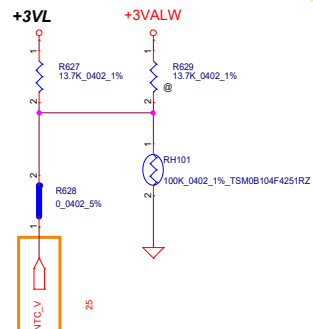


Nuvoton thermal sensor

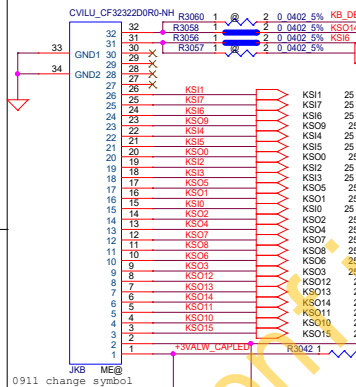
Address 1001_100xb



REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"



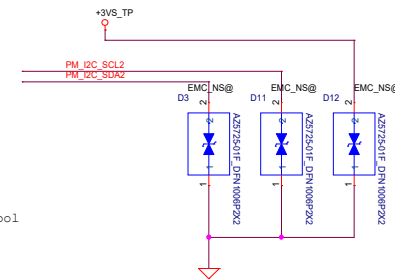
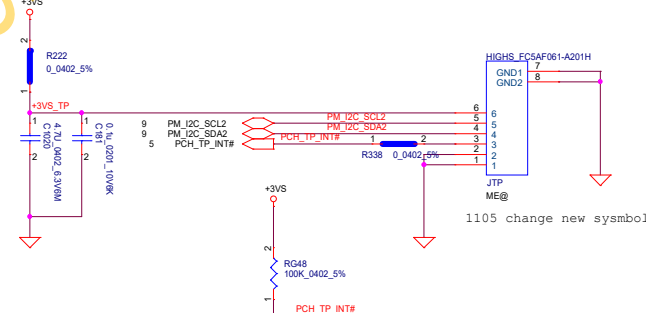
Keyboard Connector



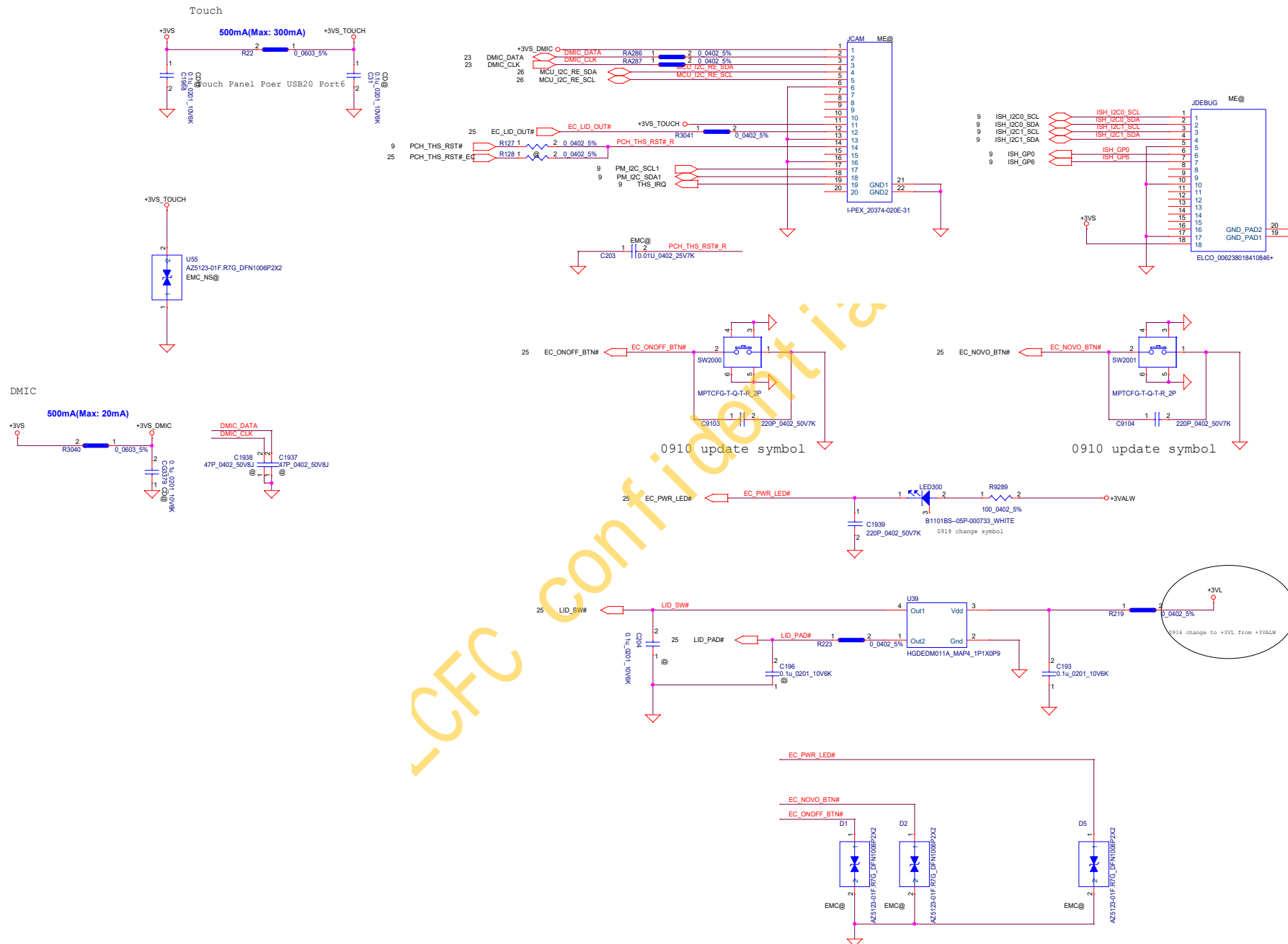
25	+3VALW_CAPLED	C117	1	2	EMC_NS@	100P_0402_50V8J	EC_CAPS_LED#	C133	1	2	EMC_NS@	100P_0402_50V8J
	KSO2	C90	1	2	EMC_NS@	100P_0402_50V8J	KSO1	C90	1	2	EMC_NS@	100P_0402_50V8J
	KSO15	C92	1	2	EMC_NS@	100P_0402_50V8J	KSO7	C93	1	2	EMC_NS@	100P_0402_50V8J
	KSO6	C94	1	2	EMC_NS@	100P_0402_50V8J	KSO2	C95	1	2	EMC_NS@	100P_0402_50V8J
	KSO8	C96	1	2	EMC_NS@	100P_0402_50V8J	KSO5	C97	1	2	EMC_NS@	100P_0402_50V8J
	KSO11	C98	1	2	EMC_NS@	100P_0402_50V8J	KSO3	C99	1	2	EMC_NS@	100P_0402_50V8J
	KSO12	C1971	1	2	EMC_NS@	100P_0402_50V8J	KSO14	C109	1	2	EMC_NS@	100P_0402_50V8J
	KSO11	C119	1	2	EMC_NS@	100P_0402_50V8J	KSO7	C110	1	2	EMC_NS@	100P_0402_50V8J
	KSO10	C107	1	2	EMC_NS@	100P_0402_50V8J	KSO6	C122	1	2	EMC_NS@	100P_0402_50V8J
	KSO3	C116	1	2	EMC_NS@	100P_0402_50V8J	KSO5	C108	1	2	EMC_NS@	100P_0402_50V8J
	KSO4	C115	1	2	EMC_NS@	100P_0402_50V8J	KSO4	C123	1	2	EMC_NS@	100P_0402_50V8J
	KSO10	C121	1	2	EMC_NS@	100P_0402_50V8J	KSO9	C1972	1	2	EMC_NS@	100P_0402_50V8J
	KSO6	C124	1	2	EMC_NS@	100P_0402_50V8J	KSO1	C120	1	2	EMC_NS@	100P_0402_50V8J

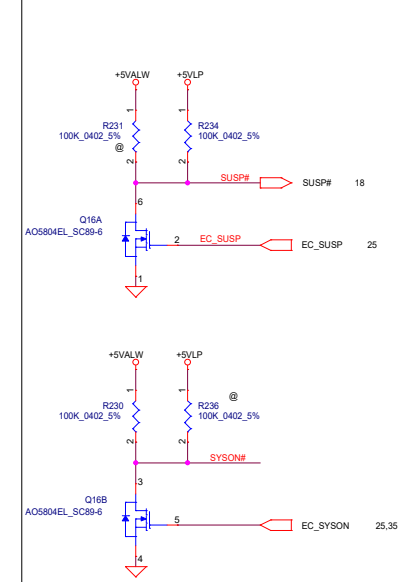
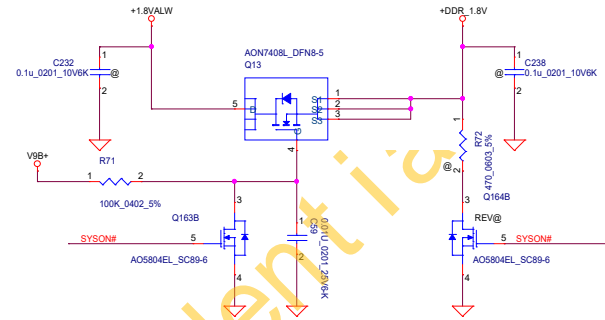
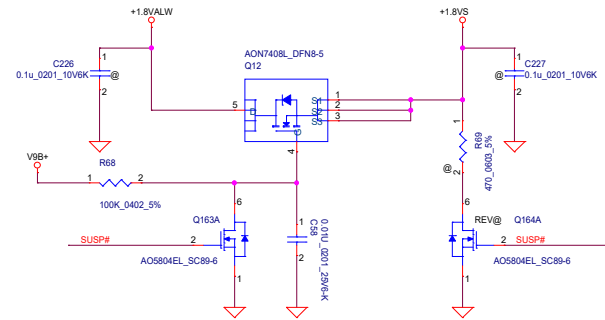
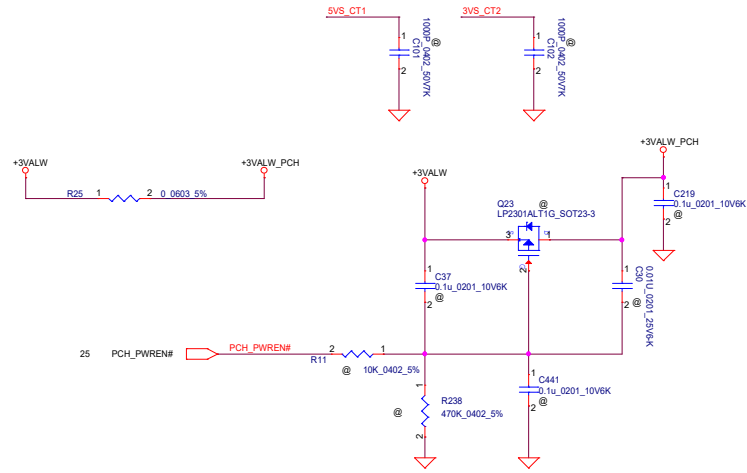
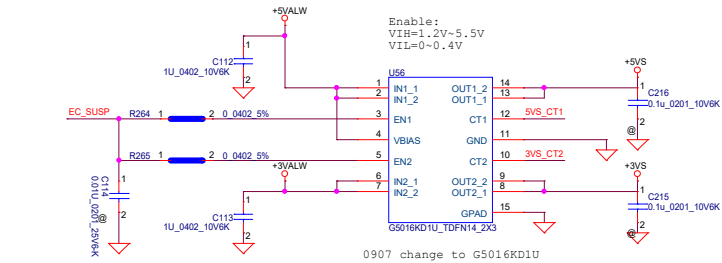
For EMC

Touch Pad Connector

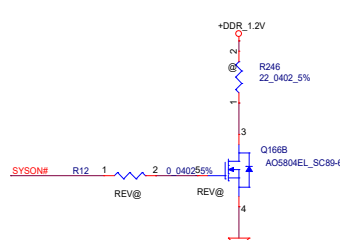
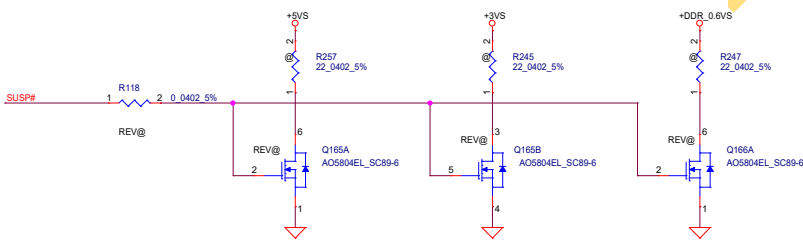


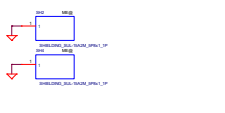
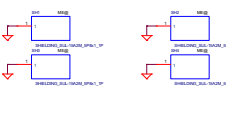
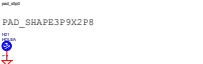
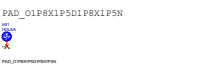
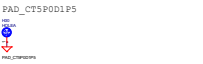
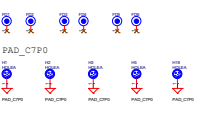
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For HDMI signal cross moat concern.




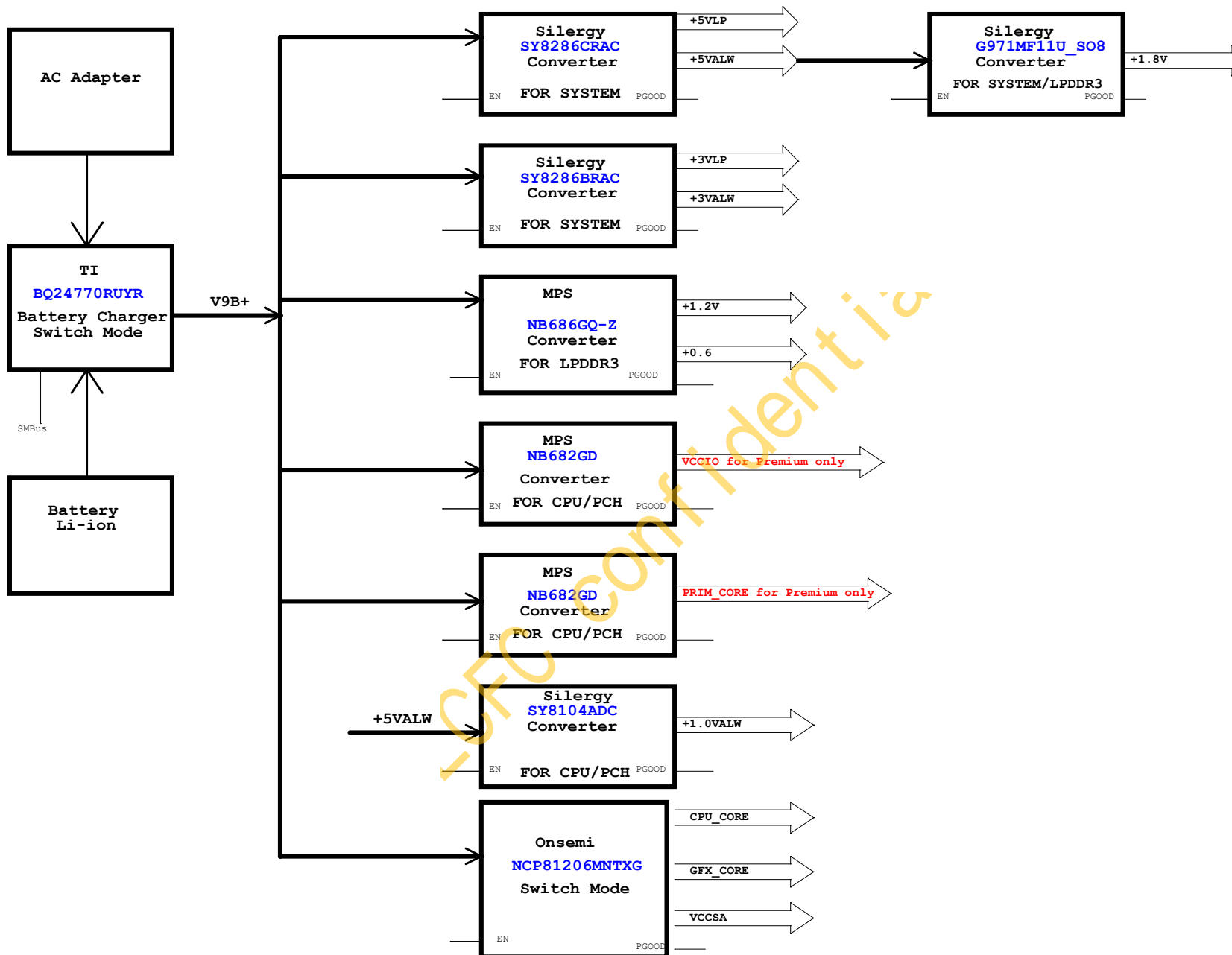


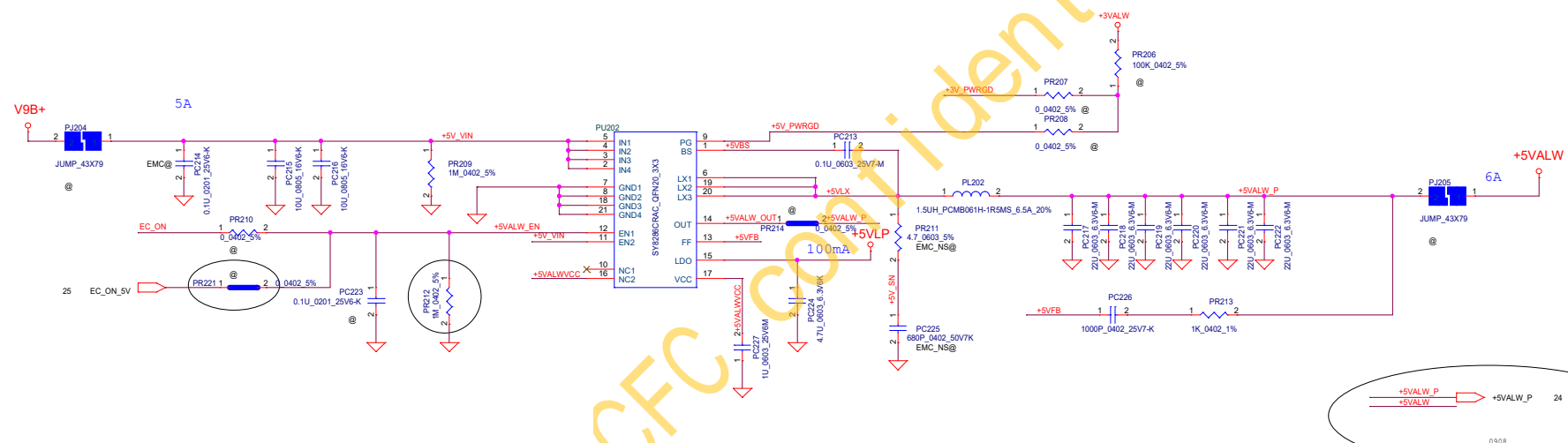
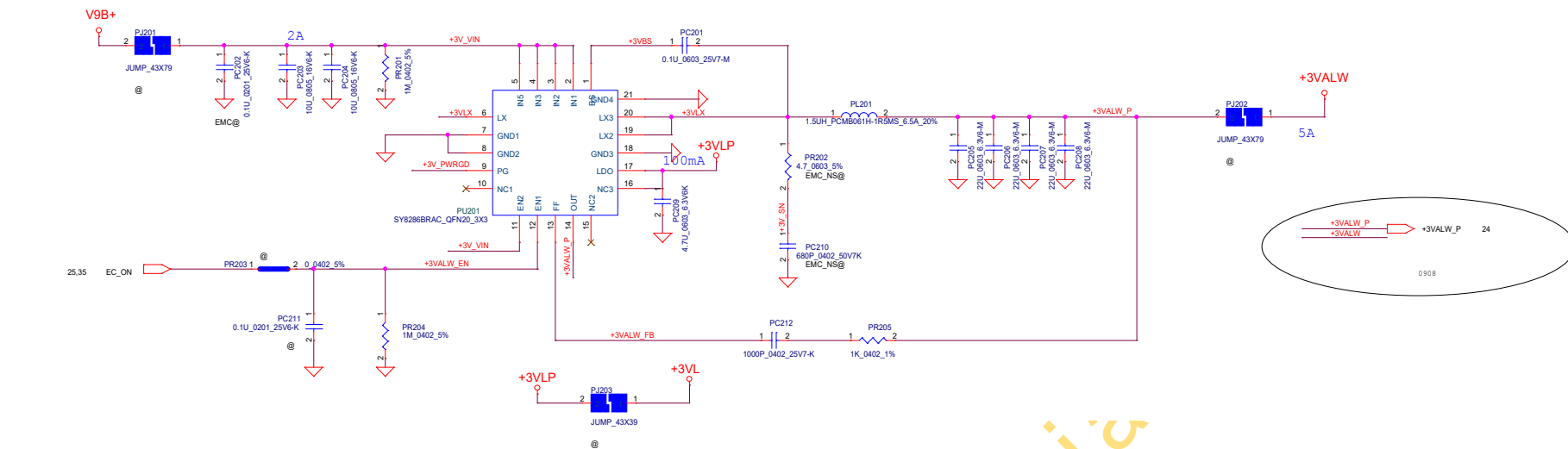
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8.31
Follow DXF update Hole

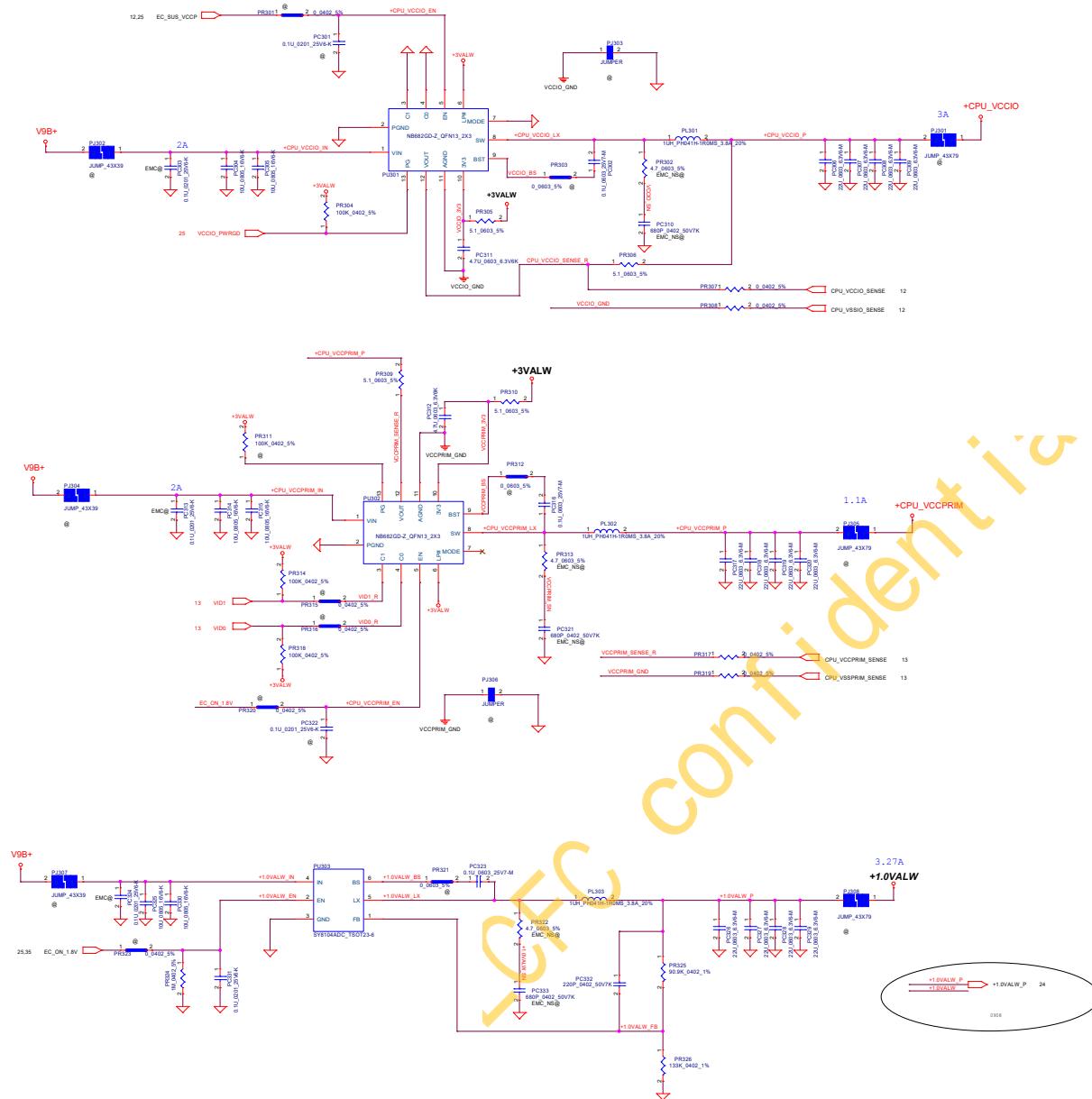
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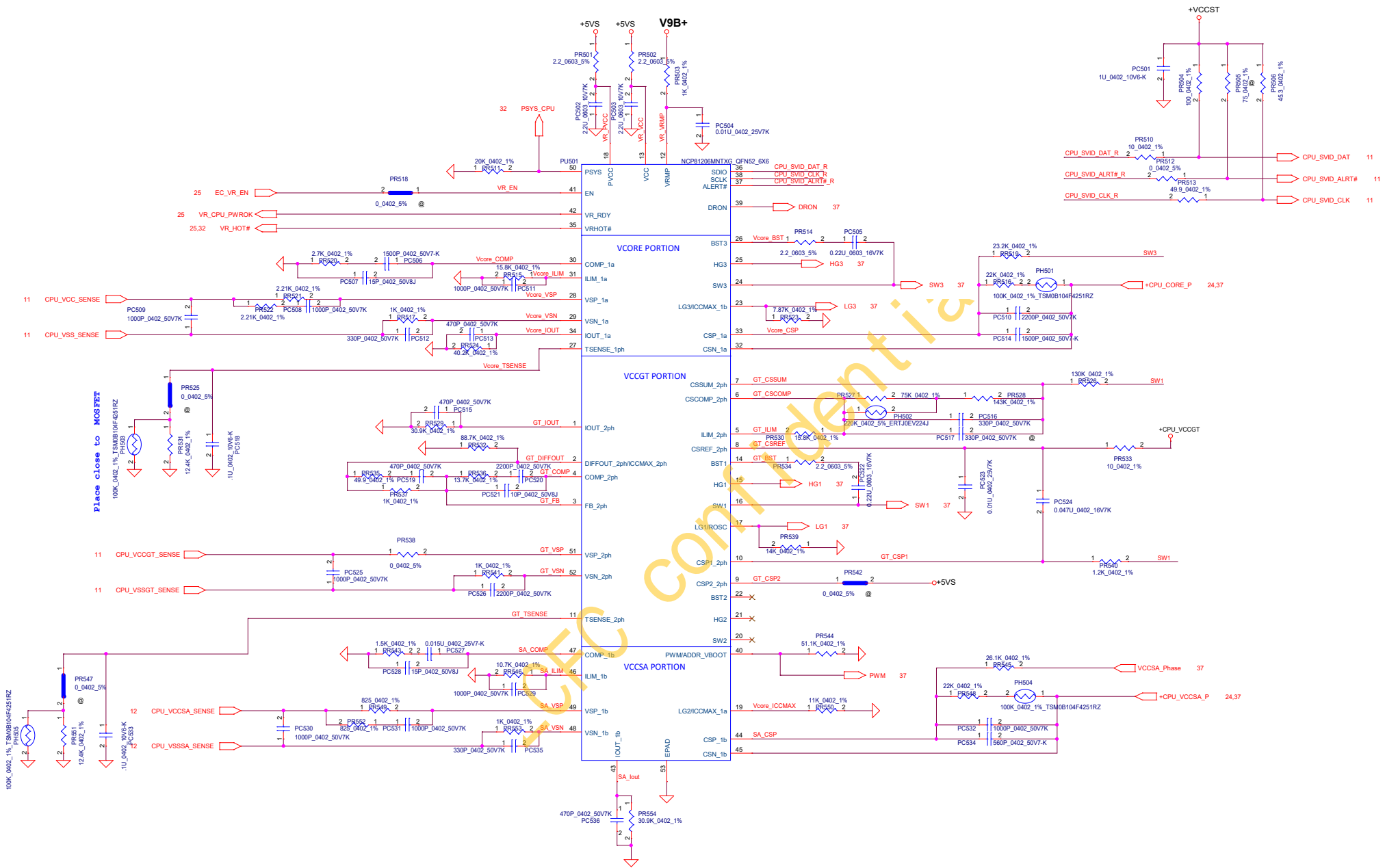
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